ABSTRACT OF THE DISCLOSURE

For erasing a block 0, a voltage Vpp is applied to select word lines WL0 - WL31, while a voltage Vneg is applied to each of the substrate (well) and sub-bit lines SBL0 - SBL4096. Also, a voltage Vneg is applied to word lines WL32 - WL63 of a non-select block 1, while the voltage Vneg is applied to the substrate (well) and the sub-bit lines SBL. Thus, the voltage Vneg is applied to the control gates, sources and drains of all the memory cells within the non-select block 1 and the substrate (well), so as to make them equal in voltage to one another. Therefore, there occur no mis-reads during the reading. Further, the capacity between the non-select word lines WL and the substrate (well) can be neglected, and the occupancy ratio of the charge pump for use of supply of the negative voltage can be reduced by an extent corresponding to 90% or more of the conventional counterpart. As a result, mis-reads due to substrate disturb during the erasing can be prevented.